Investor Update May 2021

Highlights since our last update in January include:

1) The company has opened an office in Oslo with two new employees
2) We have added another provisional patent and two more are in flight
3) We continue to make steady technical progress and the technical outlook remains good

Full Time Staff in Oslo: A new office was opened in Oslo on May 1. Joining us there is Olle Fredrikson (Senior Software Engineer) and Daniel Cuervo (Senior Software Engineer). Daniel has a PhD from University of Antwerp and brings a strong background in combinatorial optimization and constraint solvers. Olle has a PhD in computer Science from the University of Birmingham (with emphasis on programming languages) and brings a strong background in compilers and knowledge of the industry standard LLVM compiler framework.

Patents:

We have filed one new provisional patent to secure protection for our recent innovations. This patent is:
App. No. 63/166,298: Parallel Processing Architecture Using Speculative Encoding

Technical Progress:

Compiler: We continue to focus on improving the Quality of Results (QOR) of the compiler, to refine the underlying microarchitecture, and we continue to make steady progress on our Key Performance Indicators:

a) Compile time
b) Compiled image size
c) IPCW (the equivalent number of x86 **I**nstructions worth of work Per Aptos **C**ontrol **W**ord)

The team is working on introducing next stage compiler optimizations such as software pipelining, loop fusion and code fusion.

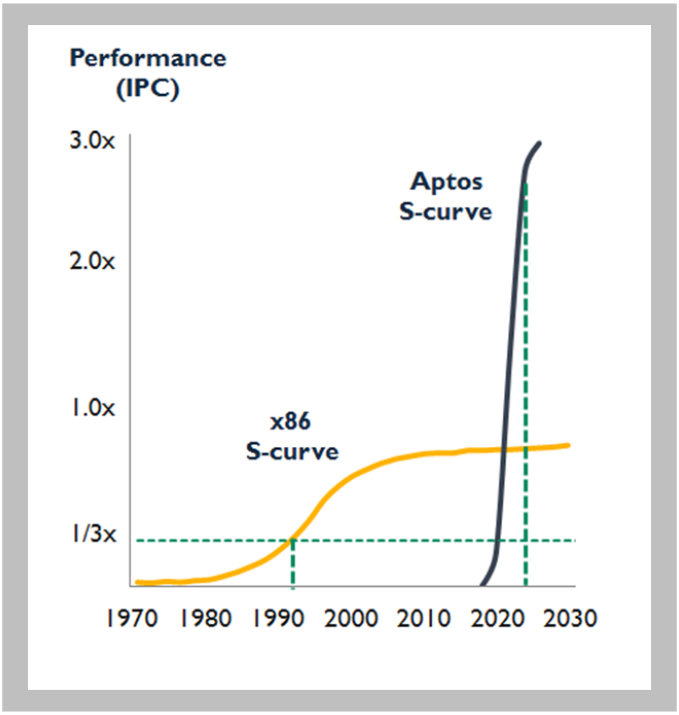
Compile Time and Compiled Image Size: As reported in our last update, compile time and compiled image size are no longer considered as potentially gating commercial viability, so we no longer report them.

IPCW: IPCW is the x86 **I**nstruction equivalent amount of computational work performed **P**er **C**ontrol **W**ord (CW). IPCW has been doubling roughly every 3 months. We measure IPCW by compiling the industry standard Coremark benchmark and executing that on our FPGA based implementation of Aptos. Our current IPCW value has more than doubled since our last update to 1.1.

To convert IPCW to IPCe (Instructions Per Cycle Equivalent), we must factor in the efficiency of the silicon implementation, i.e. an average, how many CWs can be executed per cycle. Our current estimate of this number is 0.75, which would give us a IPCe of 0.825. Once we achieve an IPCW of 3, using the 0.75 architectural efficiency value we will approach the effective IPC of existing state-of-the-art Intel processors.

Company Progress - the Big Picture:

To put Ascenium's development approach in context - we conceptually contrast the development curve for single threaded integer performance of high-end x86 processors vs that for Aptos.



The steep part of the S-curve for the x86 processors occurred from 1985 through 2003, during the period when Moore's law was in full effect and Intel designers were able to "load up" on hardware complexity (transistors) to increase performance, with little cost, power or performance penalties. During this period performance grew at 50%/yr, roughly doubling every 20 months. Performance improvement started to drop off in 2004 and until 2011 grew at a more modest 25% rate per year. However in 2012 things "fell off a cliff" in terms of single-threaded single-core performance improvement (with the demise of Moore's Law), and designers moved to multi-core designs to run multiple threads (i.e. programs) on the chip at the same time. This corresponds to the period when the S-curve reached its shoulder and we now see single-threaded single-core performance increases at an improvement plateau of ~5%/yr.

In contrast, Ascenium's approach leverages much simpler novel hardware along with a compiler that does more of the work ahead of time to much more rapidly climb the S-curve. Our goal is to provide 3x the single-core single-thread performance of x86 on a sustainable basis, protected by a unique defensible first mover patent position.

Pete